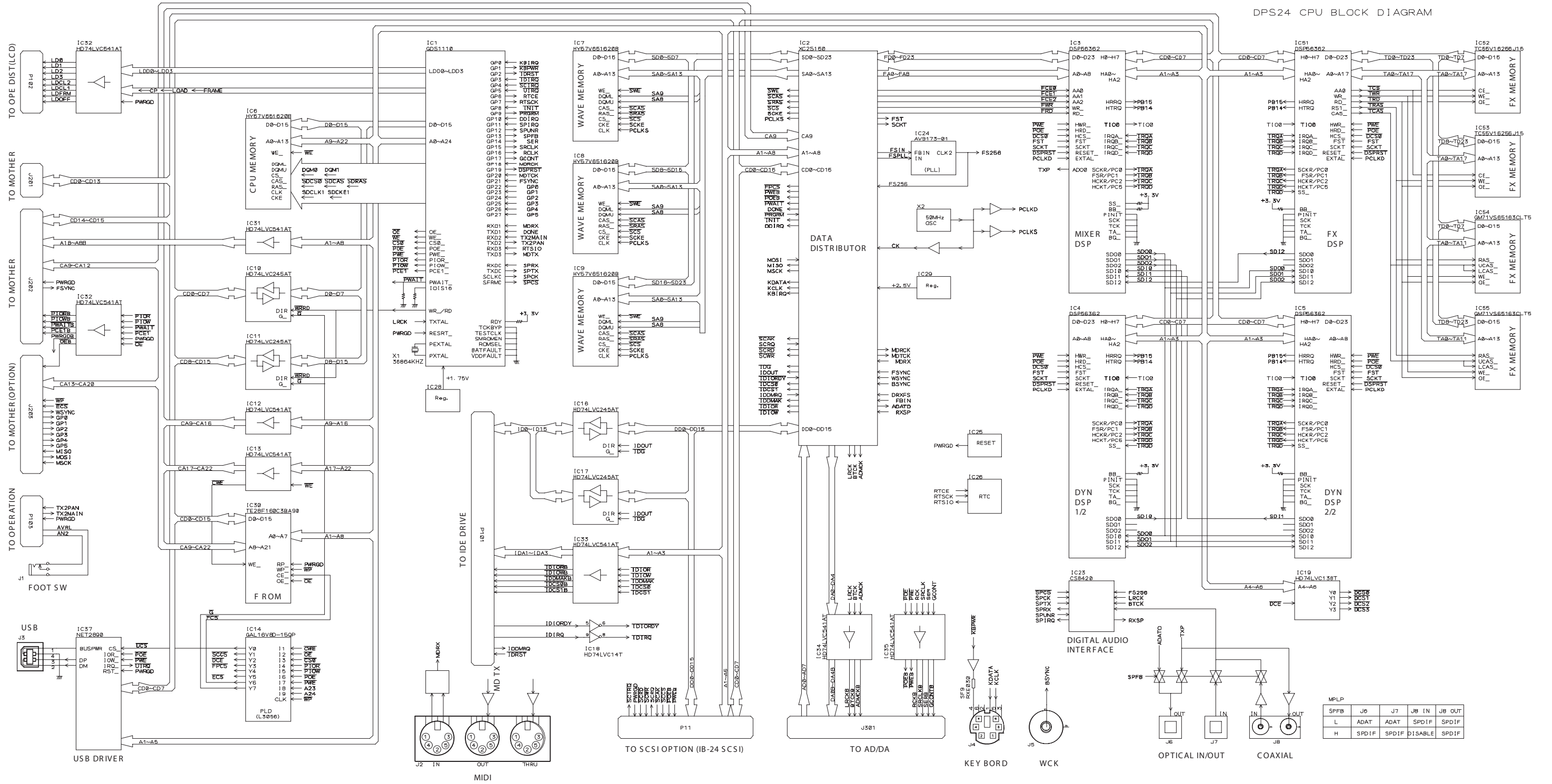


DPS24 CPU BLOCK DIAGRAM



MFLP					
SPFB	J6	J7	J8 IN	J8 OUT	
L	ADAT	ADAT	SPDIF	SPDIF	
H	SPDIF	SPDIF	DISABLE	SPDIF	